6E7104

Total No. of Questions : 22 Total No. of Pages : 04

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6E7104

B.Tech. VI-Sem. (Main/Back) Exam. May - 2025

ARTIFICIAL INTELLIGENCE AND DATA SCIENCE

6AID4-04 Computer Architecture and Organization

CS, IT, AID, CAI, CDS, CCS, CIT, CSD

Time : 3 Hours **Maximum Marks : 70**

Instructions to Candidates :

Attempt all ten questions from Part-A, five questions out of seven questions from Part-B and three questions out of five questions from Part-C.

Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used / calculated must be stated clearly.

Use of following supporting material is permitted during examination.

(Mentioned in Form No. 205)

1. ..... 2. .....

PART-A [10x2=20]

(Answer should be given up to 25 words only)

All questions are compulsory

Q.1. What is a priority interrupt?

Q.2. What are the most common fields of an Instruction format?

Q.3. What is immediate addressing mode?

Q.4. What are the major characteristics of a pipeline?

Q.5. Define latency time.

Q.6. Explain fixed point representation.

Q.7. Define multi-processing.

Q.8. Represent $(70)_{10}$ in a signed magnitude format and one's complement form.

Q.9. Write a quick note on subroutine.

Q.10. Define superscalar processor.

PART-B [5x4=20]

(Analytical/Problem solving questions)

Attempt any five questions

Q.1. Explain the functional units of an architecture of computer with diagram.

Q.2 Why interprocess synchronization needed? Explain.

Q.3. What are logical microoperatios? Explain about applications of logical microoperation.

Q.4. Differentiate between hardwired and microprogrammed control unit.

Q 5. Explain about serial communication.

Q.6. Explain the need of cache memory. Also explain Hit Ratio.

Q.7. Describe the algorithm for integer division with suitable example.

PART-C

[3x10=30]

(Descriptive/Analytical/Problem Solving/Design questions)

Attempt any three questions

Q1. Define parallel processing and explain the Flynn's classification of computer with suitable diagram.

Q.2 Explain different types of computer registers with common bus system with a neat diagram.

Q.3 Explain the Booth Algorithm with its flowchart. Perform multiplication of (-13) and (+9) using Booth Algorithm.

Q.4 What is DMA? Draw the Block diagram of DMA controller and explain it.

Q. 5. (i) How many 128×8 RAM chips are needed to provide a memory capacity of 2048 bytes?

(ii) How many lines of address bus must be used to access 2048 bytes of memory? How many of these lines will be common to all chips?

(iii) How many lines must be decoded for chip select?

(iv) Specify the size of the decoders?

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